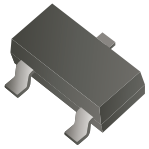
MOSFET

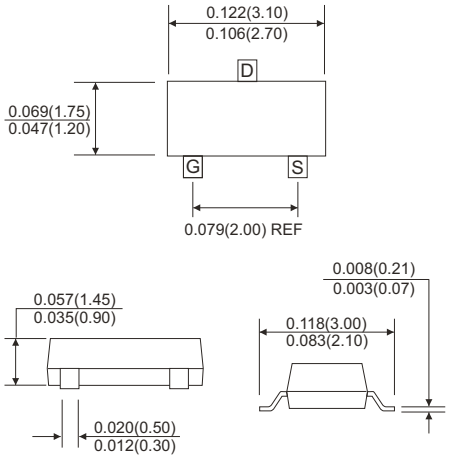
CMS2302-HF

N-Channel
RoHS Device
Halogen Free



$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
20V	55mΩ @ 4.5V	3.6A
	75mΩ @ 2.5V	

SOT-23



Dimensions in inches and (millimeter)

Features

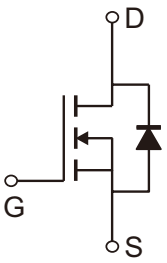
- Advanced high cell density trench technology.
- Super low gate charge.
- Excellent CdV/dt effect decline.
- Green device available.

Mechanical data

- Case: SOT-23, molded plastic.

Circuit Diagram

- G : Gate
- S : Source
- D : Drain



Description

The CMS2302 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the small power switching and load switch applications.
The CMS2302 meet the RoHS and Green Product requirement with full function reliability approved.

Maximum Ratings (at Ta=25°C unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain-Source voltage	V_{DS}	20	V
Gate-Source voltage	V_{GS}	±12	V
Continuous drain current[1], V_{GS} @ 4.5V	I_D @ T_A=25°C	3.6	A
	I_D @ T_A=70°C	2.8	A
Pulsed drain current[2]	I_{DM}	14.4	A
Power dissipation[3]	P_D @ T_A=25°C	1.0	W
Operating junction and storage temperature range	T_J, T_{STG}	-55 ~ +150	°C

Thermal Data

Parameter	Symbol	Max. Value	Unit
Thermal resistance junction-ambient [1]	$R_{\theta JA}$	125	°C/W

Electrical Characteristics (at T_A=25°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source breakdown voltage	BV_{DSS}	20			V	V_{GS}=0, I_D=250μA
Gate threshold voltage	$V_{GS(th)}$	0.4		1.2	V	V_{DS}=V_{GS}, I_D=250μA
Forward transconductance	g_{fs}		10		S	V_{DS}=5V, I_D=3A
Gate-Source leakage current	I_{GSS}			±100	nA	V_{GS}= ±12V
Drain-Source leakage current (T_J=25°C)	I_{DSS}			1	μA	V_{DS}=16V, V_{GS}=0
Drain-Source leakage current (T_J=55°C)				5		V_{DS}=16V, V_{GS}=0
Static drain-source on-resistance [2]	$R_{DS(ON)}$			55	mΩ	V_{GS}=4.5V, I_D=3A
				75		V_{GS}=2.5V, I_D=2A
Total gate charge [2]	Q_g		4.6		nC	I_D=3A V_{DS}=15V V_{GS}=4.5V
Gate-Source charge	Q_{gs}		0.7			
Gate-Drain (“Miller”) change	Q_{gd}		1.5			
Turn-on delay time [2]	$T_{d(on)}$		1.6		ns	V_{DS}=10V I_D=3A V_{GS}=4.5V R_G=3.3Ω
Rise time	T_r		42			
Turn-off delay time	$T_{d(off)}$		14			
Fall time	T_f		7			
Input capacitance	Ciss		310		pF	V_{GS}=0V V_{DS}=15V f=1.0MHz
Output capacitance	Coss		49			
Reverse transfer capacitance	Crss		35			

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode forward voltage [2]	V_{SD}			1.2	V	I_S=1A, V_{GS}=0V, T_J=25°C
Continuous source current [1, 4]	I_S			3.6	A	V_G=V_D=0V, Force Current

Notes: 1. Surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Typical Characteristic

Fig.1 - Typical Output Characteristics

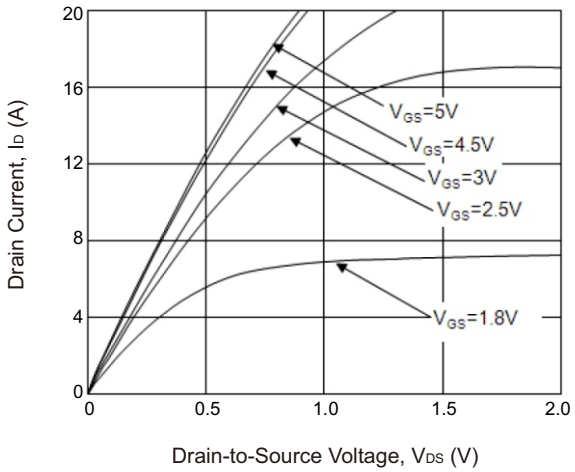


Fig.2 - On-Resistance vs.G-S Voltage

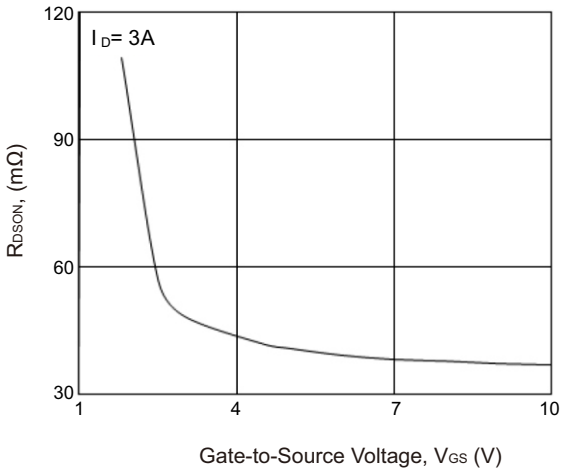


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

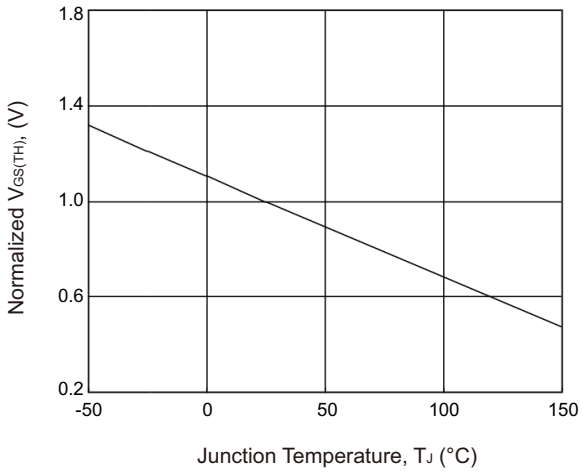


Fig.4 - Normalized R_{DSON} vs. T_J

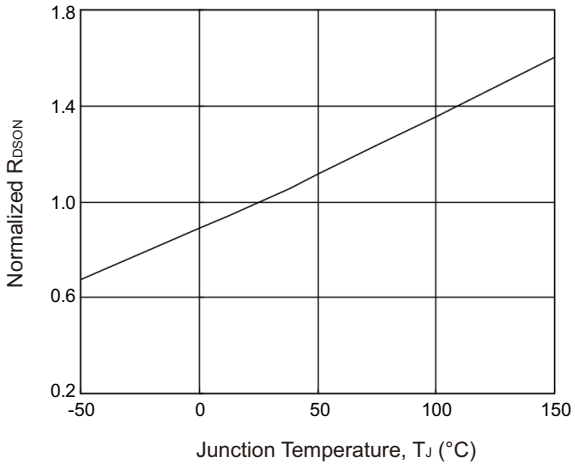


Fig.5 - Safe Operating Area

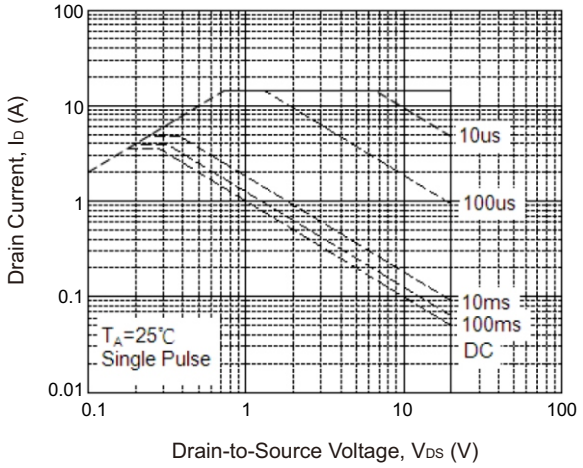


Fig.6 - Forward Characteristics of Reverse

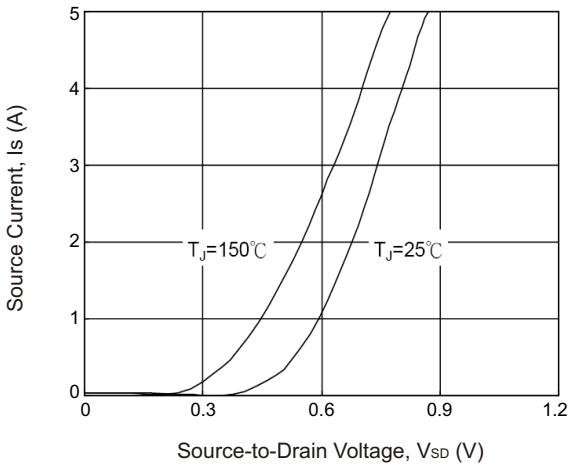


Fig.7 - Gate Charge Characteristics

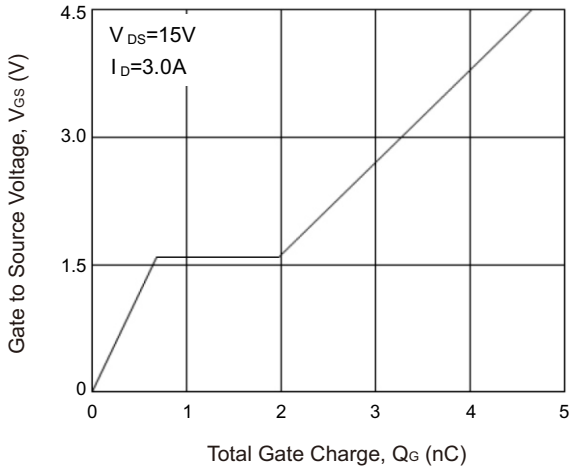


Fig.8 - Capacitance Characteristics

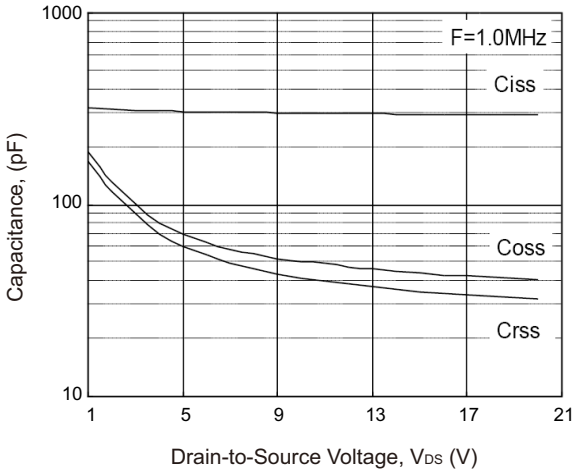


Fig.9 - Normalized Maximum Transient Thermal Impedance

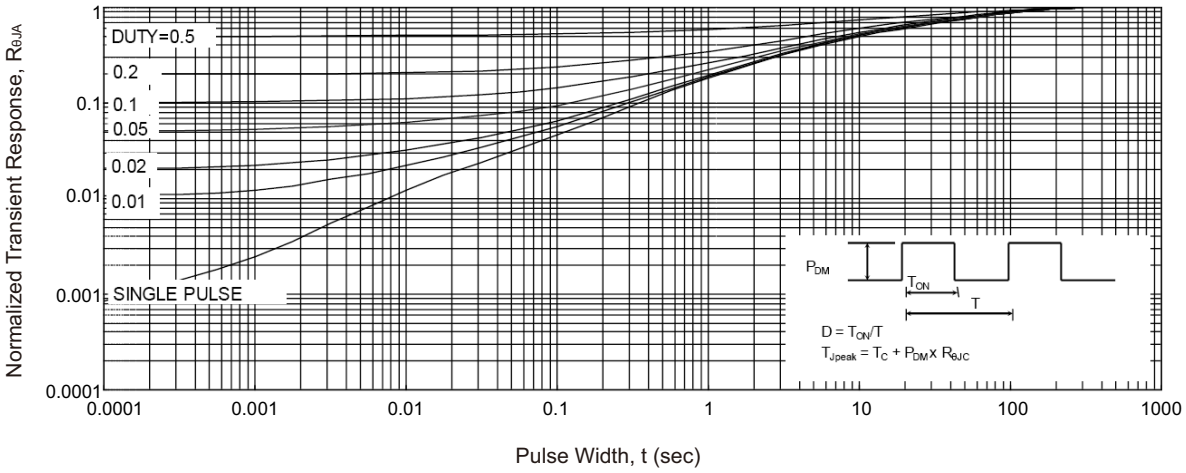


Fig.10 - Switching Time Waveform

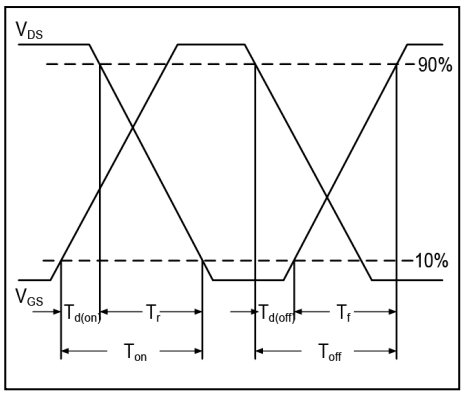
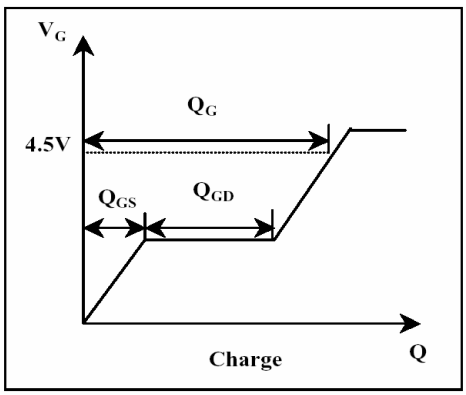
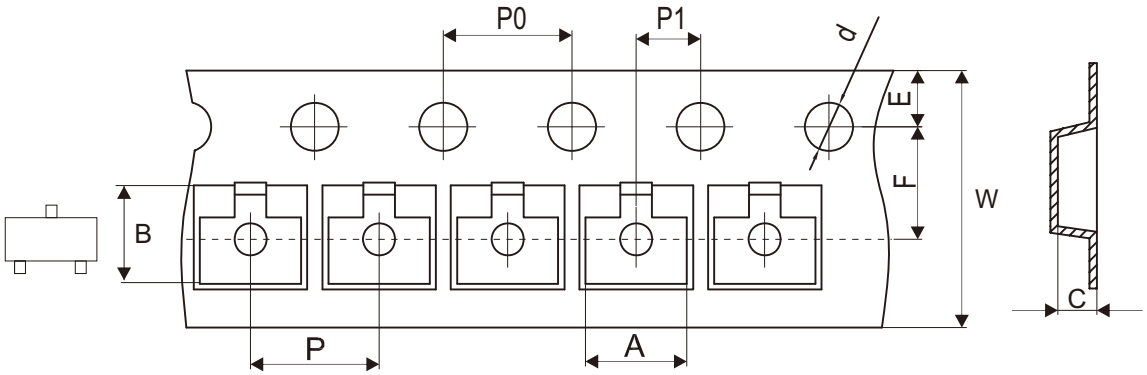
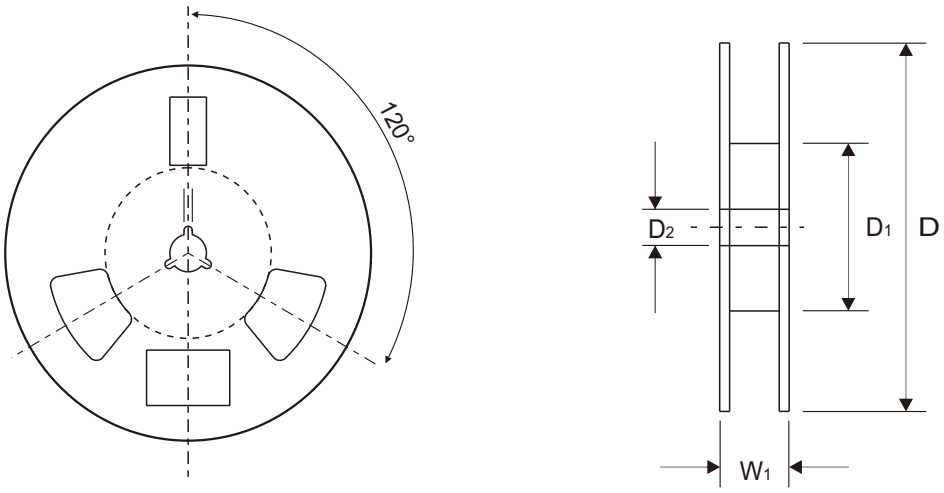


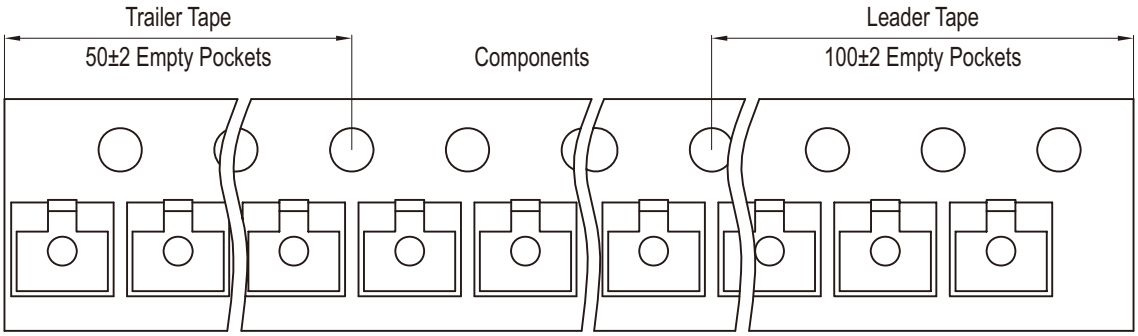
Fig.11 - Gate Charge Waveform



Reel Taping Specification







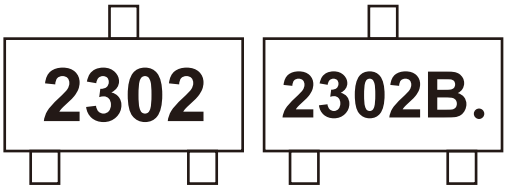
	SYMBOL	A	B	C	d	D	D1	D2
SOT-23	(mm)	See Note 1			1.50 + 0.10 − 0.00	330.00 Max.	50.00 Min.	13.00 ± 0.50
	(inch)				0.059 + 0.004 − 0.000	12.992 Max.	1.969 Min.	0.512 ± 0.020

	SYMBOL	E	F	P	P0	P1	W	W1
SOT-23	(mm)	1.75 ± 0.10	3.50 ± 0.05	4.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	8.30 Max.	14.40 Max.
	(inch)	0.069 ± 0.004	0.138 ± 0.002	0.157 ± 0.004	0.157 ± 0.004	0.079 ± 0.004	0.327 Max.	0.567 Max.

Note: 1. A, B, and C are determined by component size. The clearance between the components and the cavity must be within 0.05mm min. to 0.50mm max.

Marking Code

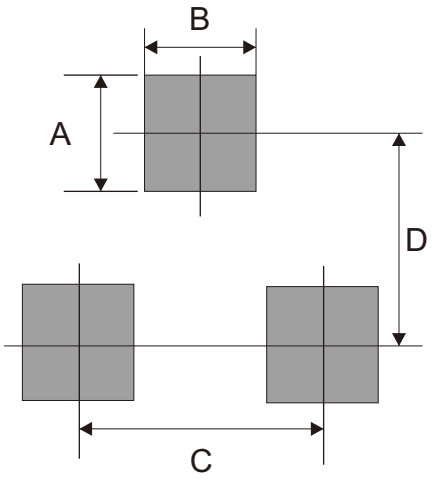
Part Number	Marking Code	
CMS2302-HF	2302	2302B.



Solid dot = Control code

Suggested P.C.B. PAD Layout

SIZE	SOT-23	
	(mm)	(inch)
A	0.80	0.031
B	0.60	0.024
C	1.90	0.075
D	2.02	0.080



Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
SOT-23	3,000	7